IN THE CLAIMS:

Claim 1. (Currently amended) A semiconductor memory device comprising:

a memory array including a plurality of memory cells arranged in a matrix;

a refresh timer circuit providing a refresh request signal at a time interval required to refresh data held by said plurality of memory cells;

a command generation circuit generating an internal command signal ~~according~~ in response to an access command; and

a row selection control circuit carrying out an operation associated with row selection of said memory array ~~according to said internal command signal and said refresh request signal~~, said row selection control circuit including

a timing control circuit rendered active ~~according~~ in response to said internal command signal to output a timing signal of a row selection operation of said memory cell,

a refresh control circuit receiving and holding said refresh request signal to output an internal refresh command signal when said timing control circuit attains an inactive state, and

a refresh timing control circuit rendered active ~~according~~ in response to said internal refresh command signal to output said timing signal instead of said timing control circuit; and

a row selection circuit carrying out row selection of said memory cell ~~according~~ in response to said timing signal.

Claim 2. (Original) The semiconductor memory device according to claim 1, wherein said access command includes a read out command,

wherein a basic cycle time starting from reception of said access command by said semiconductor memory device up to reception of the next access command is at least a total time of a normal read out cycle time starting from output of said internal command signal up to completion of data read out from said memory array and a refresh cycle time starting from output of said internal refresh command signal up to completion of refresh of a portion in said memory array corresponding to said internal refresh command signal. (fig 3)

A1 cont.

Claim 3. (Original) The semiconductor memory device according to claim 2, wherein said refresh control circuit comprises

a latch circuit receiving and holding said refresh request signal, and

a pulse generation circuit generating a pulse that becomes a basis of said internal command signal when an output of said latch circuit indicates input of said refresh request signal and said timing control circuit is rendered inactive.

Claim 4. (Original) The semiconductor memory device according to claim 2, wherein said command generation circuit holds said access command, and waits for inactivation of said refresh timing control circuit to output said internal command signal when said refresh timing control circuit is active.

Claim 5. (Original) The semiconductor memory device according to claim 4, wherein said command generation circuit comprises

a latch circuit receiving and holding said access command, and

a pulse generation circuit providing a pulse that becomes a basis of said internal command signal when an output of said latch circuit indicates input of said access command and when said refresh timing control circuit is rendered inactive.

A1 cont.

Claim 6. (Currently amended) The semiconductor memory device according to claim 2, wherein said command generation circuit comprises

an internal command generation circuit providing a command generation reference signal ~~according~~ in response to said access command, and

a delay circuit delaying said command generation reference signal for at least said refresh cycle time and providing said internal command signal,

wherein said refresh control circuit receives and holds said refresh request signal to output said internal refresh command signal when said timing control circuit attains an inactive state.

Claim 7. (Original) The semiconductor memory device according to claim 6, wherein said refresh control circuit comprises

a latch circuit holding said refresh request signal, and

a pulse generation circuit providing a pulse that becomes a basis of said internal refresh command signal when an output of said latch circuit indicates input of said refresh request signal and when said timing control circuit attains an inactive state.

Claim 8. (Original) The semiconductor memory device according to 2, further comprising a data input/output control circuit receiving and holding as read out data the output from said memory array, and receiving an output enable signal to output said read out data.

Claim 9. (Currently amended) The semiconductor memory device according to claim 2, wherein said row selection control circuit further comprises

an address latch circuit holding an applied row address to output a normal row address,

a refresh counter circuit sequentially updating and providing a refresh row address corresponding to a row to be refreshed, and

a select circuit receiving said normal row address and said refresh row address to output one of said normal row address and said refresh row address as an address corresponding to row selection of said memory array ~~according~~ in response to said internal refresh command signal.

Claim 10. (Original) The semiconductor memory device according to claim 9, wherein said memory array includes a plurality of banks that allows a row select operation independently,

wherein said refresh control circuit outputs said internal refresh command signal after said refresh control circuit is rendered inactive when a bank indicated by said normal row address coincides with a bank indicated by said refresh row address.

Claim 11. (Original) The semiconductor memory device according to claim 9, wherein said address latch circuit receives said applied row address in synchronization with a clock signal.

Claim 12. (Original) The semiconductor memory device according to claim 2, further comprising a latch circuit receiving said access command in synchronization with a clock signal and providing said access command to said command generation circuit. (col. 8; lines 24-30)

Al concl'd

Claim 13 - Claim 17. (Withdrawn)